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Docket No.: SCEI 3.0-086
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Nobuo Sasaki

Application No.: 09/964,247 Group Art Unit: 2151

Filed: September 26, 2001 Examiner: Not Yet Assigned

For: MULTI-PROCESSOR SYSTEM, DATA PROCESSING SYSTEM, DATA PROCESSING METHOD, AND COMPUTER PROGRAM

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

CERTIFICATION PURSUANT TO 37 C.F.R. § 197(E)(1)

Sir:

Pursuant to 37 C.F.R. § 1.97(e) (1), undersigned counsel hereby certifies that each item of information contained in the accompanying Information Disclosure Statement was cited in a communication from a foreign patent office in a counterpart foreign application to the above-referenced patent application not more than three months prior to the filing of said statement.

Dated: May 23, 2003

Respectfully submitted,

By _____
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LD-456\

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INFORMATION DISCLOSURE STATEMENT

Sir:

It is respectfully requested that the Official Action issued February 25, 2003 in connection with applicant's corresponding Japanese patent application, along with its English translation, be made of record and considered with respect to the above-referenced U.S. patent application. A copy of each is enclosed. The references cited in the Official Action have been made of record in an Information Disclosure Statement previously submitted in connection with this application. Submission of the present Information Disclosure Statement should not be taken as an admission that the cited reference is legally available prior art or that the same is pertinent or material.

In the event that any fee is due in connection with the present Information Disclosure Statement, the Commissioner is hereby authorized to charge the same to our Deposit Account No. 12-1095.

Dated: May 23, 2003

Respectfully submitted,

By _____

Robert B. Cohen
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LD-458\

Reference No.: SCEI01111 Dispatch No.: 062084
Dispatch Date: February 25, 2003

Notification of Reason(s) of Rejection (Translation)

Application Number	2001-289588	
Drafting Date	February 21, 2003	
Examiner	Yasushi SEIKI	9643 5B00
Representative	Seigoh SUZUKI, et al.	
Provision(s) Applied	Patent Law Sections 29(2), 36 and 37	

This application should be rejected by the following reasons. If the applicant disagree with the rejection, the applicant can file an argument within 60 days from the dispatch date of this notification.

Reasons

Reason 1

A patent should not be granted under 29(2), because the invention according to the claims set forth below of the present application would have been readily invented, prior to the filing thereof, by a person of ordinary skill in the art to which the invention pertains on the basis of the inventions set forth in the following publications publicly available in Japan or abroad prior to the filing thereof.

Note (For the cited references, see the List of Cited References.)

· Claims: 1, 2, 3, 4, 7, 8, 10, 11, 12, 13, 14, 15 and 16
· Cited References: 1, 2, 3 and 4
· Comments

Cited Reference 1 discloses an invention wherein each of a plurality of processors selects only data necessary for data processing performed by the processor from broadcast data, processes the data, and writes the result of the data processing back to the shared memory (page 1, lower right column, line 12 to page 2, upper right column, line 17; Figs. 1-2).

A content code communication approach is well known to those of ordinary skill in the art, where a content code indicative of the content of data is appended to the data communicated, so that each processor on the receiving end determines whether it is

receivable or not based on the content code (Cited Reference 2: page 3, lower left column, line 8 to page 4, upper left column, line 6; page 5, upper left column, lines 2-16; Figs. 1-3).

Cited Reference 3 discloses an invention wherein a multiprocessor system includes a collection circuit (which corresponds to the "WTA/sum circuit" of the present application) that performs data selection or data addition for data outputted from a plurality of processors PE (for example, processor number or output data from a processor) and outputs the results thereof (for example, processor numbers selected, output data selected, or sum of output data from all the processors) to the controller; this collection circuit achieves bus arbitration among each of the processors, determination of maximum or minimum value of output data from each processor, and summing of output data from all the processors.

It is a well-known technique for a person of ordinary skill in the art to provide to a multiprocessor system a ring bus that establishes a connection between adjacent processors (Cited Reference 4: paragraphs 0026-0027; Fig. 1).

All of the inventions and well-known technique disclosed in Cited References 1-4 are related to a multiprocessor system. Thus, it is not difficult to apply the well-known technique disclosed in Cited Reference 2 to the broadcast in the invention disclosed in Cited Reference 1, to apply the invention disclosed in Cited Reference 3 for bus arbitration and summing operation as post-processing after data processing by each processor in the invention disclosed in Cited Reference 1, and to employ the well-known technique disclosed in Cited Reference 4 for communication between adjacent processors in the invention disclosed in Cited Reference 1.

· Claim: 9

· Cited References: 3 and 5

· Comments

Cited Reference 5 discloses an invention wherein a plurality of individual pattern patching sections have respective distributed identification dictionaries with different standard patterns as their registered content (which correspond to "template data" of the present application), and pattern matching for identifying a standard pattern that is most approximate to a single input pattern, i.e., "distance" is shortest, is performed by the plurality of individual pattern matching sections in a distributed manner.

In the invention of Cited Reference 5, comparison processing (processing to determine a minimum value among the processors) for a value of "distance" of the

multiple individual pattern matching sections is conducted by a host pattern matching section. It is not difficult to apply the collection circuit in the invention of Cited Reference 3 (which has a similar objective to determine a minimum value of output data for the respective processors) to the invention of Cited Reference 5 and redesign it so that the processing to determine the minimum value among the processors is performed by dedicated hardware (not the host pattern matching section) regarding the processing to determine the minimum value among the processors.

Reason 2

This application does not meet the requirements set forth in 37.

Note

Principal portions of the invention according to claims 1, 10, 12, 13, 14, 15, and 16 are such that each of a plurality of processors selects only data necessary for data processing performed by the processor from broadcast data, and processes the data. On the other hand, a principal portion of the invention according to claim 9 is such that the processors hold respective sets of template data different from one another and compare the broadcast input data with the template data. It cannot be said that those principal portions are the same. In addition, the problems to be solved cannot also be said to be identical.

Thus, the invention according to claim 9 does not meet the requirement for unity of invention, relative to the invention according to the other claims.

(Although claims 14-16 do not have clear description regarding selection of data by the processors receiving broadcast data, unity of invention was recognized as if they had similar purport to claim 1. Note that, however, if the descriptions in claims 14-16 do not imply selection of data by the processors receiving broadcast data, it seems that the invention according to claims 14-16 also do not meet the requirement for unity of invention, relative to the invention according to claim 1.)

Reason 3

This application does not meet the requirements set forth in 36(6)(i).

Note

Referring to claims 14-16, it is unclear what the applicant intends to claims by "broadcast data including identification information for the identified data processing

means and data for data processing addressed to that data processing means." In the specification and drawings, the "data processing means" pointed by the "identification information" in the above description and the "data processing means" that is to receive the "broadcast data" including the "identification information" attached thereto are not necessarily the same. Thus, claims 14-16 are rejected as being indefinite.

Reason 4

This application does not meet the requirements set forth in 36(6)(ii).

Note

Referring to claim 16, it is not clear what the applicant intends to claim by "semiconductor device", and what it corresponds to in the embodiment described in the specification and drawings.

No reason of rejection is found for the claims not specified in this notification. If any new reason for rejection is found, the applicant will be notified of same accordingly.

List of Cited References

1. JP2-47757
2. JP3-62255
3. JP2-81258
4. JP7-84966
5. JP61-283976

Result of Search for prior art

Field Searched	IPC(7)	G06F15/16-15/177
		G06T 1/00- 1/40
		G06N 1/00- 7/08
		G06F17/10-17/18
		G06T 3/00- 9/40
		G06K 9/00-9/82
		G06F17/30

Name of Data Base

Prior art Document(s)

This record is not component(s) of the reason(s) of rejection.

Any inquiry concerning this notification or request for an interview should be directed to Yasushi SEIKI whose telephone number is 03-3581-1101 (ext. 3545) and facsimile number is 03-3501-0737.